CLAIMS:

What is claimed is:

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1. A method for removing polymer etch residue from an etched opening in a silicon wafer device comprising contacting said opening with ammonia gas to remove said polymer etch residue.

2. The method of claim 1, wherein said opening is a High Aspect Ratio (HAR) contact opening.

3. The method of claim 2, wherein said contacting is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.

4. The method of claim 3, wherein said opening is contacted with ammonia gas in the absence of oxygen.

5. The method of claim 2, wherein said ammonia gas is in a plasma.

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6. The method of claim 5, wherein said contacting is done at a temperature within the range of about 250 - 500° C.

7. The method of claim 6, wherein said contacting is performed in a plasma reactor within a power reactor range of about 500 - 2500 watts.

8. The method of claim 7, wherein said contacting is performed within a power range of about 1500 - 2000 watts.

9. The method of claim 7, wherein said contacting is performed with an ammonia gas flow rate within the range of about 500 to 1000 SCCM.

10. The method of claim 9, wherein said contacting is performed at power of about 1900 watts and a temperature of about 350°C.

11. The method of claim 10, wherein said contacting is performed with an ammonia gas flow rate of about 750 SCCM.

12. The method of claim 9, wherein said contacting is performed for a period of less than about 100 seconds.

13. The method of claim 12, wherein said contacting is performed for a period of not more than about 75 seconds.

14. The method of claim 1, further comprising forming a conductive layer at the bottom of said opening following said contacting step.

15. The method of claim 5, wherein said contacting step produces silicon nitride at the bottom of said opening, said method further comprising removing said silicon nitride.

16. A method for removing polymer etch residue from an etched opening in a silicon wafer device, comprising the steps of:

contacting said opening with an oxygen containing plasma, stopping said oxygen plasma contacting before said polymer etch residue is

completely removed and thereafter contacting said opening with ammonia gas.

17. The method of claim 16, wherein said contact opening is an High Aspect Ratio (HAR) opening, and said ammonia contacting step is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.

18. The method of claim 17, wherein said ammonia contacting occurs in the absence of oxygen.

19. The method of claim 18, wherein said ammonia gas is in a plasma.

20. The method of claim 19, wherein said ammonia contacting is performed at a temperature within the range of about 250 - 500° C.

21. The method of claim 19, wherein said ammonia contacting is performed in a reactor operating in a power range of about 500 - 5000 watts.

22. The method of claim 20, wherein said ammonia contacting is performed at a temperature of about 350°C.

23. The method of claim 21, wherein said reactor power is about 1900 watts.

24. The method of claim 21, wherein said ammonia contacting is performed at a flow rate within the range of about 100 to 4000 SCCM.

25. The method of claim 15, wherein said ammonia contacting is performed for a period of time sufficient to remove said residue from a bottom of said opening.

26. The method of claim 25, wherein said bottom of said opening is not oxidized during said ammonia contacting step.

27. The method of claim 24, wherein said contacting is performed for a period of less than about 100 seconds.

28. The method of claim 27, wherein said contacting is performed for a period of not more than about 75 seconds.

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29. A method of forming a contact opening in a semiconductor device, comprising:

a) etching a contact opening in an insulative layer in said device down to a polysilicon element of said device; and

b) cleaning etch residue from said etched opening by contacting said opening with ammonia gas.

30. The method of claim 29, wherein said contacting is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.

31. The method of claim 30, wherein said contacting is performed under conditions which do not oxidize said opening.

32. The method of claim 31, wherein said opening is contacted in the absence of added oxygen.

33. The method of claim 30, wherein said ammonia gas is in a plasma.

34. The method of claim 33, wherein said contacting is done in a plasma reactor at a temperature within the range of about 250 - 500° C, with a reactor power within the range of about 500 – 2500 watts, with an ammonia gas flow rate of about 500 to 1000 SCCM, and for a period of no more than 100 seconds.

35. The method of claim 34, wherein said contacting is performed within a reactor power range of about 1500 - 2000 watts.

36. The method of claim 34, wherein said contacting is performed with a reactor power at about 1900 watts and a temperature of about 350°C.

37. The method of claim 34, wherein said contacting is performed with an ammonia gas at a flow rate of about 750 SCCM.

38. The method of claim 35, wherein said contacting is performed for a period of not more than about 75 seconds.

39. The method of claim 29, further comprising forming a silicide layer at the bottom of said contact opening following said contacting operation.

40. The method of claim 29, further comprising contacting said opening with an oxygen plasma between said etching and cleaning steps to remove a portion of said etch residue.

41. The method of claim 29, wherein an insulating layer is formed on said device prior to said etching and said etching forms a contact hole in said insulating layer.

42. The method of claim 41, wherein said etching is dry etching.

43. The method of claim 42, wherein said dry etching is performed using at least one fluorine-containing gas.

44. The method of claim 43, wherein said fluorine-containing gas is at least one gas selected from the group consisting of CH_2F_2, CHF_3, C_2F_6, C_2HF_5, and CH_3F.

45. A semiconductor device comprising:

an insulating layer; and

an ammonia-cleaned etched opening in said insulating layer; and,

a conductor formed in said cleaned opening.

46. An integrated circuit comprising an ammonia-cleaned, etch residue-free High Aspect Ratio opening provided in an insulating layer, said opening being formed atop a polysilicon region, said opening containing a conductor which electrically connects with said polysilicon region.

47. An integrated circuit as in claim 46 further comprising:

a silicide layer between said conductor and said polysilicon region.

48. An integrated circuit as in claim 46, wherein said integrated circuit is a memory circuit.

49. An integrated circuit as in claim 47 wherein the interface area between said conductor and polysilicon region is free of oxygen contamination.

50. A method of forming an integrated circuit structure comprising:

forming an insulating layer over a polysilicon region;

forming a high aspect ratio contact opening in said insulating layer down to said polysilicon region using a fluorine containing gas;

removing polymer residue from said contact opening using a gas which provides an oxide free bottom of said contact opening;

forming a silicide layer at the bottom of said opening in contact with said polysilicon layer;

forming a conductor in said opening in electrical contact with said silicide layer.

51. A method as in claim 50 wherein said gas for removing said polymer residue is ammonia gas.

52. A method as in claim 50 further comprising removing a potion of said polymer residue from said contact opening with oxygen prior to using said gas which provides an oxide free bottom of said contact opening.

53. A method as in claim 50 wherein said silicide layer is a titanium silicide layer.